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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,902	08/02/2001	Masahiko Watanabe	35.C15650	4530

5514 7590 05/13/2003

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EXAMINER	
NGUYEN, LAM S	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 05/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,902	WATANABE, MASAHIKO	
	Examin r	Art Unit	
	LAM S NGUYEN	2853	

-- Th MAILING DATE of this communicati n appears on th cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-17* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Applicant's arguments, see REQUEST FOR RECONSIDERATION, filed 04/29/2003, with respect to the rejection(s)of claim(s) 1-17 under Hoshino (JP 2001-100873) have been fully considered and are persuasive. Therefore, the Final Rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kobayashi et al. (US 5583987).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 7/1-4, 10-13, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al. (US 5583987).

Kobayashi et al. disclose an integrated-circuit apparatus comprising:

a CPU (in term of "master CPU") (FIG. 16, element 5a) and a plurality of circuit blocks (in term of "slave CPUs) (FIG. 16, elements 5b-5d) (column 2, line 4-14) to be initialized in accordance with external reset signals (column 1, line 55-60), wherein

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized (column 2, line 38-43),

the CPU outputs an enable signal for permitting operations of the circuit blocks in

accordance with the initialization completion signals output from the circuit blocks (column 2, line 21-24: the slave CPUs 5b-d wait for an enable signal given from the master CPU 5a and column 2, line 44-49: after the master CPU 5a receives the completion report from the slave CPUs, the apparatus 1 including the slave CPUs 5b-5d starts its operation), and

the circuit blocks are permitted to perform the operations by the enable signal (column 2, line 21-24: the slave CPUs 5b-d wait for an enable signal given from the master CPU 5a) and the external reset signals (column 1, line 55-66).

Referring to claim 2: wherein the circuit blocks are initialized to output the initialization completion signals, and said apparatus further comprises a logic circuit for inputting the initialization completion signals output from the circuit blocks to logic-operate the signals, and outputting the logic-operation results to the CPU (column 15, line 60-64: Because the master CPU resets the slave CPUs at one time, there exists a logic circuit receiving all initialization completion signals from the slave CPUs and outputting one signal to the master CPU, so the master CPU knows when all the slave CPUs complete the initialization to reset them at one time).

Referring to claims 3, 4: wherein when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit blocks (column 2, line 21-24: the slave CPUs 5b-d wait for an enable signal given from the master CPU 5a and column 2, line 44-49: after the master CPU 5a receives the completion report from the slave CPUs, the apparatus 1 including the slave CPUs 5b-5d starts its operation).

Referring to claim 7/1-4: wherein the circuit blocks output the initialization completion

signals when a predetermined period passes after the reset signal is input (column 4, line 14-20: the time out).

Referring to claims 10-13: wherein the integrated-circuit apparatus is used for a printer (Because these claims are the apparatus claims, the recited intended use of the integrated circuit apparatus does not differentiate the claims from the structure of the apparatus disclosed by Kobayashi et al. (MPEP 2114: *A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claims*)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8/1-4 and 9/7/1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (US 5583987) in view of Mitani (US 5929672).

Kobayashi et al. disclose the claimed invention as discussed above except wherein the integrated-circuit apparatus is constituted of one chip.

However, Mitani discloses a power on reset circuit including a CPU and the circuit blocks (FIG. 4) that is constituted of one chip (column 5, line 23-26).

Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to constitute the CPU and the circuit blocks as disclosed by Kobayashi et al. in one chip as taught by Mitani. The motivation of doing so is to avoid unwanted reset signal for resetting internal circuits of a semiconductor device due to the momentarily voltage drops during a normal operation affected by a noise as taught by Mitani (column 2, line 21-45).

3. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al. (US 5784080) in view of Kobayashi et al. (US 5583987).

Nitta et al. discloses an ink-jet recording apparatus (column 1, line 17) comprising an integrated-circuit apparatus for controlling recording (FIG. 4) by a recording head, wherein the integrated-circuit apparatus comprises a CPU (FIG. 4, element 55), a plurality of circuit blocks (FIG. 4, elements 57, 59), a control circuit (FIG. 4), and a driving circuit for performing the recording (FIG. 4, element 53) (**Referring to claim 16**). However, Nitta et al. does not disclose the circuit blocks initialized in accordance with external reset signals and each respectively outputs an initialization completion signal for communicating completion of initialization or for initializing the control circuit or the driving circuit (**Referring to claims 15-16**) after the circuit blocks are initialized, and the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks.

Kobayashi et al. disclose an apparatus having CPU and circuit blocks initialized in accordance with external reset signals (column 1, line 55-63), the circuit blocks each respectively outputs an initialization completion signal (column 2, line 38-42) for communicating completion of initialization or for initializing the control circuit or the driving circuit after the circuit blocks

are initialized, the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks (column 2, line 21-24 and column 2, line 44-49).

Therefore, it would have been obvious for one having ordinary skill in the art at the time the invention was made to modify the initialization process of the electronic device used in the printer disclosed by Nitta et al. such that the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization and the CPU outputs an enable signal to permit operations of the circuit blocks in accordance with the initialization completion signals as disclosed by Kobayashi et al. The motivation of doing so is to be able to detect the fault circuit blocks or the fault CPU during the initialization thereby stopping the setting-up process of the system as taught by Kobayashi et al. (column 257 to column 3, line 3).

Allowable Subject Matter

3. Claims 5, 6, 7/5-6, 8/5-6, 9/7/5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claims 5, 6, 7/5-6, 8/5-6, 9/7/5-6: The most pertinent arts Nitta et al. (US 5784080), Mitani (US 5929672), and Kobayashi et al. (US 5583987) fail to disclose wherein if there is any circuit block that is not initialized yet, the CPU initializes the circuit block by using the enable signal. Therefore, the claimed invention is not disclosed in the cited prior arts.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S NGUYEN whose telephone number is (703)305-3342. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RUSS ADAMS can be reached on (703)308-2847. The fax phone numbers for the organization where this application or proceeding is assigned are (703)305-3431 for regular communications and (703)305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

LN
May 7, 2003

Judy Nguyen
JUDY NGUYEN
PRIMARY EXAMINER